WHAT IS CLAIMED:

1. A method of forming a metal layer in an integrated circuit device, the method comprising:

forming a recess in a surface of an insulating layer, the recess having a side wall inside the recess, a bottom inside the recess, and an edge at a boundary of the surface of the insulating layer and the side wall;

forming a selective electroplating mask on the side wall to provide a covered portion of the side wall and to provide an exposed portion of the side wall that is free of the selective electroplating mask; and

electroplating a metal on the exposed portion of the side wall.

2. A method according to Claim 1 wherein forming a selective electroplating mask comprises forming the selective electroplating mask on the surface adjacent to the edge and on the side wall adjacent to the edge and not on the side wall beyond adjacent to the edge.

3. A method according to Claim 1 wherein electroplating comprises electroplating the metal on the exposed portion of the side wall and on the bottom to fill the recess with the metal to beneath a level of the electroplating mask on the side wall.

4. A method according to Claim 1 wherein forming a recess further comprises forming the recess to a depth that is about at least three times as great as a width of the recess.

5. A method according to Claim 4 wherein the width is in a range between about 0.05 μm and about 0.7 μm and the depth is in a range between about 0.2 μm and about 5 μm.

6. A method according to Claim 4 wherein forming a selective electroplating mask comprises forming an oxide layer on the insulating layer and the recess using sputtering or reactive vapor deposition.

7. A method according to Claim 6 wherein forming an oxide layer comprises forming the oxide layer to a thickness in a range between about 10 Ångstroms and about 500 Ångstroms.

8. A method according to Claim 4 wherein the insulating layer comprises a first insulating layer, wherein forming a selective electroplating mask comprises forming a second insulating layer on the first insulating layer and on the recess using plasma enhanced chemical vapor deposition.

9. A method according to Claim 4 wherein forming a selective electroplating mask comprises:

forming a metal layer on the first insulating layer and on the recess; and

oxidizing the metal layer.

10. A method according to Claim 1 wherein forming a recess is followed by:

forming a trench in the surface of the insulating layer on the recess that is wider than the recess, wherein the trench exposes the edge of the recess.

11. A method according to Claim 1 wherein the metal comprises a first metal, the method further comprising:

forming a second metal on the first metal.

12. A method according to Claim 1 wherein the metal comprises copper.

13. A method according to Claim 1 further comprising:

avoiding forming the selective electroplating mask on the covered portion of the side wall.

14. A method of forming a metal layer in an integrated circuit device, the method comprising:

etching a recess in a surface of an insulating layer, the recess having a side wall inside the recess, a bottom inside the recess, and an edge at a boundary of the surface of the insulating layer and the side wall;

etching a trench in the surface of the insulating layer on the recess that is wider than the recess, wherein the trench exposes the edge of the recess;

forming a barrier metal layer in the recess and in the trench and on the insulating layer;

forming a seed layer on the barrier metal layer;

forming a selective electroplating mask on the seed layer on the side wall adjacent to the edge to provide a covered portion of the side wall and not on the side wall beyond adjacent to the edge to provide an exposed portion of the side wall;

forming a first metal in the recess to beneath a level of the electroplating mask on the exposed portion of the side wall and not on the covered portion of the side wall;

forming a second metal in the recess and in the trench on the first metal and on the selective electroplating mask; and

planarizing the second metal layer to expose the selective electroplating mask.

15. A method according to Claim 14 wherein the barrier metal layer comprises a first barrier metal layer, wherein the seed layer comprises a first seed layer, wherein forming a first metal in the recess is followed by:

forming a second barrier metal layer in the trench on the first metal; and

forming a second seed layer in the trench on the second barrier metal layer.

16. A method according to Claim 14 wherein forming a selective electroplating mask comprises forming an oxide layer to a thickness in a range between about 10 Ångstroms and about 500 Ångstroms.

17. A method according to Claim 14 wherein forming a barrier metal layer comprises forming the barrier metal layer to a thickness in a range between about 100 Ångstroms and about 700 Ångstroms using IPVD or CVD.

18. A method according to Claim 14 wherein forming a seed layer comprises forming the seed layer to a thickness in a range between about 50 Ångstroms and about 2500 Ångstroms using IPVD or CVD.

19. A method according to Claim 14 wherein a width of the recess is in a range between about 0.05 μm and about 0.7 μm and the depth is in a range between about 0.2 μm and about 5 μm.

20. A method according to Claim 14 wherein forming a selective electroplating mask comprises forming an oxide layer on the insulating layer and the recess using sputtering or reactive vapor deposition.

21. A method of forming a metal layer in an integrated circuit device, the method comprising:

etching a first recess in a surface of a first insulating layer, the first recess having a first side wall inside the first recess, a first bottom inside the first recess, and a first edge at a boundary of the surface of the first insulating layer and the first side wall;

forming a first barrier metal layer in the first recess and on the surface of the first insulating layer;

forming a first seed layer on the first barrier metal layer;

forming a first selective electroplating mask on the first seed layer on the first side wall adjacent to the first edge to provide a covered portion of the first side wall and not on the first side wall beyond adjacent to the first edge to provide an exposed portion of the first side wall;

forming a first metal on the exposed portion of the first side wall in the first recess and that protrudes beyond the first recess and not on a portion of the first selective electroplating mask on the surface of the first insulating layer spaced apart from the first edge;

planarizing the first metal to expose the first selective electroplating mask on the first edge;

forming a second insulating layer on the first metal;

etching a surface of the second insulating layer to form a second recess that exposes the first metal, the second recess having a second side wall inside the second recess, a second bottom inside the second recess, and a second edge at a boundary of the surface of the second insulating layer and the second side wall;

forming a second barrier metal layer in the second recess and on the surface of the second insulating layer;

forming a second seed layer on the second barrier metal layer;

forming a second selective electroplating mask in the second recess on the second side wall adjacent to the second edge to provide a covered portion of the second side wall and not on the second side wall beyond adjacent to the second edge to provide an exposed portion of the second side wall;

forming a second metal in the second recess and on a portion of the second selective electroplating mask adjacent to the second edge and that protrudes beyond the second recess and not on a portion of the second selective electroplating mask on the surface of the second insulating layer spaced-apart from the second edge; and

planarizing the second metal to expose the second selective electroplating mask on the second edge.

22. A method according to Claim 21 wherein forming a first selective electroplating mask comprises forming an oxide layer to a thickness in a range between about 10 Ångstroms and about 500 Ångstroms.

23. A method according to Claim 21 wherein forming a first barrier metal layer comprises forming the first barrier metal layer to a thickness in a range between about 100 Ångstroms and about 700 Ångstroms using IPVD or CVD.

24. A method according to Claim 21 wherein forming a first seed layer comprises forming the first seed layer to a thickness in a range between about 50 Ångstroms and about 2500 Ångstroms using IPVD or CVD.

25. A method according to Claim 21 wherein a width of the first recess in a range between about 0.05 μm and about 0.7 μm and the depth is in a range between about 0.2 μm and about 5 μm.

26. A method according to Claim 21 wherein forming a first selective electroplating mask comprises forming an oxide layer on the insulating layer and the recess using sputtering or reactive vapor deposition.

27. A conductive contact in an integrated circuit device comprising:

a recess in an integrated circuit substrate, the recess having a side wall inside the recess, a bottom inside the recess, and an edge at a boundary of a surface of the insulating layer and the side wall;

a selective electroplating mask on the side wall adjacent to the edge to provide a covered portion of the side wall and not on the side wall beyond adjacent to the edge to provide an exposed portion of the side wall; and

an electroplated metal on the exposed portion of the side wall.

28. A conductive contact according to Claim 27 wherein the recess has a depth that is about at least three times as great as a width of the recess.

29. A conductive contact according to Claim 28 wherein the width is in a range between about 0.05 μm and about 0.7 μm and the depth is in a range between about 0.2 μm and about 5 μm.

30. A conductive contact according to Claim 27 further comprising:

a barrier metal layer in the recess between the electroplated metal and the side wall; and

a seed layer on the barrier metal layer opposite the side wall.

31. A conductive contact according to Claim 27 wherein the electroplating mask comprises at least one of an oxide of aluminum, silicon, tantalum or titanium having a thickness in a range between about 10 Ångstroms and about 500 Ångstroms.

32. A conductive contact according to Claim 30 wherein the barrier metal layer comprises at least one of tantalum, titanium, tungsten, and/or a nitride of one or more of these materials having a thickness in a range between about 100 Ångstroms and about 700 Ångstroms.

33. A conductive contact according to Claim 30 wherein the seed layer comprises at least one of copper, tungsten, platinum, or gold having a thickness in a range between about 50 Ångstroms and about 2500 Ångstroms.

34. A method for fabricating a metal layer in a semiconductor device, the method comprising:

forming an insulating layer having a concave portion on a semiconductor substrate;

forming a selective electroplating mask for exposing a portion of the conductive underlying layer, which is formed at an inside portion of the hole, and for covering at least a portion of the conductive underlying layer, which is formed at the edges of the mouth of the hole; and

selectively electroplating the inside of the concave portion that is exposed by the selective electroplating mask.

35. The method of claim 34, wherein the selective electroplating mask is formed of an insulating material.

36. The method of claim 35, wherein the selective electroplating mask is formed of a nitride or oxide made of aluminum, silicon, tantalum or titanium.

37. The method of claim 34, wherein forming the selective electroplating mask comprises:

forming a thin layer with aluminum, tantalum or titanium; and

oxidizing the thin layer.

38. The method of claim 34, wherein the metal layer is formed of copper (Cu), platinum (Pt), palladium (Pd) or nickel (Ni).

39. The method of claim 34 further comprises forming a seed layer, which is used for electroplating the metal layer, below the metal layer.

40. The method of claim 39, wherein the seed layer is formed of copper (Cu), tungsten (W), platinum (Pt) or gold (Au).

41. The method of claim 34, wherein a barrier metal layer is formed below the metal layer.

42. A method for fabricating a metal layer in a semiconductor device, the method comprising:

forming an insulating layer having a hole and a trench on a semiconductor substrate;

forming a conductive underlying layer on the insulating layer;

forming a selective electroplating mask for exposing a portion of the conductive underlying layer, which is formed inside a portion of the hole, and for covering at least a portion of the conductive underlying layer, which is formed at the edges of the mouth of the hole;

forming a first metal layer by selectively electroplating a metal layer at the inside portion of the hole, which is exposed by the selective electroplating mask; and

forming a second metal layer to fill the trench on the first metal layer.

43. The method of claim 42, wherein the selective electroplating mask comprises an insulating layer.

44. The method of claim 42, wherein the selective electroplating mask is formed of aluminum, silicon, tantalum or titanium, or a nitride or oxide made of one of these materials.

45. The method of claim 42, wherein forming the selective electroplating mask comprises:

forming a thin layer with aluminum, tantalum or titanium; and

oxidizing the thin layer.

46. The method of claim 42, wherein the first metal layer is formed of copper (Cu), platinum (Pt), palladium (Pd) or nickel (Ni).

47. The method of claim 42, wherein the conductive underlying layer comprises a seed layer for electroplating the metal layer.

48. The method of claim 47, wherein the seed layer is formed of copper (Cu), tungsten (W), platinum (Pt) or gold (Au).

49. The method of claim 42, wherein the conductive underlying layer comprises a barrier metal layer.

50. A method for fabricating a metal layer in a semiconductor device, the method comprising:

forming a first insulating layer having a hole in the first insulating layer;

forming a conductive underlying layer on the first insulating layer;

forming a selective electroplating mask for exposing a portion of the conductive underlying layer, which is formed inside a portion of the hole, and for covering at least a portion of the conductive underlying layer, which is formed at the edges of the mouth of the hole;

forming a first metal layer to fill the hole by selectively electroplating a metal layer at the inner portion of the hole that is exposed by the selective electroplating mask;

forming a second insulating layer having at least a trench, which exposes the first metal layer, on the first insulating layer; and

forming a second metal layer to fill the trench.

51. The method of claim 50, wherein the selective electroplating mask comprises an insulating material.

52. The method of claim 50, wherein the selective electroplating mask is formed of aluminum, silicon, tantalum or titanium, or a nitride or oxide made of one of these materials.

53. The method of claim 52, wherein forming the selective electroplating mask comprises:

forming a thin layer of aluminum, tantalum or titanium; and

oxidizing the thin layer.

54. The method of claim 50, wherein the conductive underlying layer comprises a seed layer for electroplating the metal layer.

55. The method of claim 50, wherein the conductive underlying layer comprises a barrier metal layer.

56. The method of claim 50 further planarizing the first metal layer until the upper surface of the first insulating layer is exposed.

57. A method for fabricating a metal layer in a semiconductor device, the method comprising:

forming a first insulating layer having a hole on a semiconductor substrate;

forming a first metal layer to fill the hole;

forming a second insulating layer having at least a trench, which exposes the first metal layer, on the first insulating layer;

forming a conductive underlying layer on the second insulating layer;

forming a selective electroplating mask for exposing a portion of the conductive underlying layer, which is formed at the inside portion of the hole, and for covering at least a portion of the conductive underlying layer, which is formed at the edges of the mouth of the hole; and

forming a second metal layer to fill the trench by selectively electroplating a metal layer only in the trench, which is exposed by the selective electroplating mask.

58. The method of claim 57 further comprising:

forming a second conductive underlying layer on the first insulating layer;

forming a selective electroplating mask for exposing a portion of the conductive underlying layer, which is formed at the inside portion of the hole, and for covering a portion of the conductive underlying layer, which is formed at the edges of the mouth of the hole; and

forming a first metal layer by selectively electroplating a metal layer only in the hole exposed by the second selective electroplating mask.

59. The method of claim 57 further comprising planarizing the second metal layer until the upper surface of the second insulating layer is exposed.

60. A method of forming a metal layer in an integrated circuit device, the method comprising:

forming a recess in a surface of an insulating layer, the recess having a side wall inside the recess, a bottom inside the recess, and an edge at a boundary of the surface of the insulating layer and the side wall;

forming a selective deposition mask on the side wall to provide a covered portion of the side wall and to provide an exposed portion of the side wall that is free of the selective deposition mask; and

depositing a metal on the exposed portion of the side wall.

61. A method according to Claim 60 wherein the depositing comprises sputtering the metal on the exposed portion of the side wall.

62. A method according to Claim 60 wherein the depositing comprises electroplating the metal on the exposed portion of the side wall.